ATME College of Engineering

Department of EEE
Emitting Elite Energy

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

Lesson Plan &Work-done Diary for AY: 2025-26, ODD Semester

Course with Code: Digital Logic Circuits / BEE306A			Faculty: Mrs. Swathi C A			Semester & Section: III	
Class No.	**Date planned (DD/MM)**	**Topics to be covered**	**TLP Planned**	**Date of Conduction (DD/MM)**	**Topics Covered**	**TLP Executed**	**Remarks if any deviation**
MODULE-1							
1		**Principles of Combinational Logic:** Definition of combinational logic	ICT				
2		Canonical forms	ICT				
3		Generation of switching equations from truth tables	ICT				
4		Karnaugh map rules & regulations	ICT				
5		Karnaugh maps-3,4,5 variables	Chalk & Talk				
6		Karnaugh maps-3,4,5 variables	Chalk & Talk				
7		Incompletely specified functions (Don ‘t care terms)	Chalk & Talk				
8		Simplifying Max term equation	Chalk & Talk				
9		Quine-McCluskey minimization technique	Chalk & Talk				
10		Quine-McCluskey using don ‘t care terms	Chalk & Talk				
11		Reduced prime implicants Tables	Chalk & Talk				

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MODULE-2							
12		**Analysis and Design of Combinational logic:** General approach to combinational logic design	Chalk & Talk				
13		Decoders and BCD decoders	Chalk & Talk				
14		Encoders	Chalk & Talk				
15		Digital multiplexers	Chalk & Talk				
16		Using multiplexers as Boolean function generators	Chalk & Talk				
17		Adders and subtractors	Chalk & Talk				
18		Cascading full adders	Chalk & Talk				
19		Look ahead carry, Binary comparators	Chalk & Talk				

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	MODULE-3						
20		**Flip-Flops:** Basic Bistable elements	Chalk & Talk				
21		Latches, Timing considerations	Chalk & Talk				
22		The master-slave flip-flops	Chalk & Talk				
23		SR flip-flops, JK flip-flops	Chalk & Talk				
24		Edge triggered flip- flops	Chalk & Talk				
25		Characteristic equations	Chalk & Talk				

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	MODULE 4						
26		**Flip-Flops Applications:** Registers	Chalk & Talk				
27		binary ripple counters, synchronous binary counters	Chalk & Talk				
28		Counters based on shift registers	Chalk & Talk				
29		Design of a synchronous counter	Chalk & Talk				
30		Design of a synchronous mod-n counter using clocked T Flip Flop	Chalk & Talk				
31		Design of a synchronous mod-n counter using clocked JK Flip Flop	Chalk & Talk				
32		Design of a synchronous mod-n counter using clocked D Flip Flop	Chalk & Talk				
33		Design of a synchronous mod-n counter using clocked SR Flip Flop	Chalk & Talk				
34		Design of asynchronous counter	Chalk & Talk				

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	MODULE 5						
35		**Sequential Circuit Design:** Mealy and Moore models	Chalk & Talk				
36		State machine notation	Chalk & Talk				
37		Synchronous Sequential circuit analysis	Chalk & Talk				
38		Construction of state diagrams	Chalk & Talk				
39		Counter design	Chalk & Talk				
40		Memories: Read only and Read/Write Memories, Programmable ROM, EPROM, Flash memory	ICT				

	Activity	Planned	Actual	Remarks
1	Theory Classes	40		
2	Assignments / Quizzes / Self study	06 (Activity - 01 SRS – 05)		
3	Tutorials / Extra classes	_		
4	Internal Assessments	03		
5	ICT based Teaching (% of usage in Curriculum)	30%		
Planning			**Execution**	
Faculty Signature:			**Faculty Signature:**	
HOD Signature:			**HOD Signature:**	