Department of Electrical and Electronics Engineering

COURSE MODULES OF THE COURSE TAUGHT FOR THE ODD SESSION AUG-DEC 2025-26

Course Syllabi with CO's

Faculty Name: **Mrs. Swathi C A**				Academic Year: **2025-26**				
Department: Electrical & Electronics Engineering								
Course Code	Course Title	Core/Elective	Prerequisite	Contact Hours				Total Hrs/ Sessions
				L	T	P	S	
BEE 306A	**Digital Logic Circuits**	**Elective**	**Basic Electronics**	**3**	**-**	**-**	**-**	**40 Hr Theory**
Objectives	• To illustrate simplification of algebraic equations using Karnaugh Maps and Quine-McClusky methods • To design decoders, encoders, digital multiplexer, adders, subtractors and binary comparators • To explain latches and flip-flops, registers and counters • To analyze Melay and Moore Models • To develop state diagrams synchronous sequential circuits • To understand the applications of sequential circuits							

Topics Covered as per Syllabus

Module-1: **8 hours**

Principles of Combinational Logic: Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don't care terms) Simplifying Max term equations, Quine-Mc Cluskey minimization technique, Quine-Mc Cluskey using don't care terms, Reduced prime implicants Tables.

Module-2: **8 hours**

Analysis and Design of Combinational logic: General approach to combinational logic design, Decoders, BCD decoders, Encoders, digital multiplexers, Using multiplexers as Boolean function generators, Adders and subtractors, Cascading full adders, Look ahead carry, Binary comparators.

Module-3: **8 hours**

Flip-Flops: Basic Bistable elements, Latches, Timing considerations, The master-slave flip-flops (pulse triggered flip-flops):SR flip-flops, JK flip-flops, Edge triggered flip- flops, Characteristic equations

Module -4: **8 hours**

Flip-Flops Applications: Registers, binary ripple counters, synchronous binary counters, Counters based on shift registers,Design of a synchronous counter, Design of a synchronous mod-n counter using clocked T, JK, D and SR flip-flops.

Module-5: **8 hours**

Sequential Circuit Design: Mealy and Moore models, State machine notation, Synchronous Sequential circuit analysis,Construction of state diagrams, counter design.
Memories: Read only and Read/Write Memories, Programmable ROM, EPROM, Flash memory.

List of Text Books and Reference Books

Text Books:

(1) John M Yarbrough , Digital logic applications and design, Thomson Learning, 2001.
(2) Donald D Givone, Digital Principles and design, MC Graw Hill 2002.
(3) Charles H Roth Jr, Larry L Kinney, Fundamentals of logic design, Cengage Learning, 7th Edition.

Reference Books:

(1) D.P.Kothari and J S Dhillon, -Digital circuits and design, Pearson, 2016.
(2) Morris Mano, Digital Design, PHI, 3rd edition.
(3) K.A. Navas, Electronics Lab Manual, Vol.1, PHI 5th edition, 2015.

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List of URLs, Text Books, Notes, Multimedia Content, etc	
1. https://onlinecourses.nptel.ac.in/noc20_ee32/preview 2. YouTube videos on digital electronics 3. National Instruments: https://education.ni.com/teach/resources/1104/digital-electronics	
Course Outcomes	At the end of the course the students will be able to: 1. **Explain** the concept of combinational and sequential logic circuits. [L2] 2. Analyse and **design** combinational circuits. [L3] 3. **Describe** and characterize flip flops and its applications. [L3] 4. **Design** the sequential circuits using SR, JK, D and T flip-flops and Melay and Moore applications. [L3] 5. **Design** applications of combinational and sequential circuits. [L3] 6. **Employ** the digital circuits for different applications. [L3]
Internal Assessment Marks: 50 (2 Theory Tests of 25Marks each + 2 Assignments of 10 Marks each are conducted during thesemester and marks allotted based on average all the performances).	

The Correlation of Course Outcomes (CO's) and Program Outcomes (PO's)

Course Code:	BEE306A	TITLE: Digital Logic Circuits					Faculty Name:	Mrs. Swathi C A					
List of Course Outcomes	Program Outcomes												
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO-1	3	2	2	-	2	-	-	-	-	-	-	-	2	-
CO-2	3	3	2	-	2	-	-	-	-	-	-	-	2	-
CO-3	2	2	2	-	-	-	-	-	-	-	-	-	2	-
CO-4	2	2	2	-	-	-	-	-	-	-	-	-	2	-
CO-5	3	3	2	-	-	-	-	-	-	-	-	-	2	-
CO-6	2	-	-	-	-	-	-	-	-	-	-	-	2	-

Note: 3 = Strong Contribution 2 = Average Contribution 1 = Weak Contribution '-'= No Contribution

Course Coordinator Vertical Head HoD