ATME College of Engineering

Department of EEE
Emitting Elite Energy

Department of Electrical & Electronics Engineering

Lesson Plan & Work-done Diary for AY:2025-26, ODD Semester

	Course with Code: Analog Electronic Circuits –BEE303				Faculty: Shreeshayana R		Semester & Section: III	
Class No.	**Date planned (DD/MM)**	**Topics to be covered**	**TLP Planned**	**Class No.**	**Date of Conduction (DD/MM)**	**Topics Covered**	**TLP Executed**	**Remarks if any deviation**
	MODULE-1							
1	15.09.2025 Monday	**Course Orientation, CO-PO mapping, Delivery Awareness, Activity Discussion.**	ICT					
2	16.09.2025 Tuesday	**Diode Circuits**: Basics, V-I Characteristics, Rectifier,	ICT					
3	18.09.2025 Thursday	Diode clipping circuits, Diode clamping circuits.	ICT + Chalk & Talk					
4	19.09.2025 Friday	**Transistor Biasing and Stabilization:** The operating point, load line analysis DC analysis and design of fixed bias circuit						
5	22.09.2025 Monday	Emitter stabilized bias circuit, Collector to base bias circuit	Chalk & Talk					
6	23.09.2025 * Tuesday	Voltage divider bias circuit, Modified DC bias with voltage feedback, Numerical solving	Chalk & Talk					
7	25.09.2025 Thursday	Bias stabilization and stability factors for fixed bias circuit, Numerical solving	Chalk & Talk					
8	26.09.2025 Friday	Collector to base bias circuit and voltage divider bias circuit, bias compensation, Transistor switching circuits, Numerical solving	ICT + Chalk & Talk					
9	29.09.2025 Monday	Summary of Module-1, VTU QP Discussion, SRS Activity	ICT					
10	03.10.2025 Friday	Group Activity-1	ICT					

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	MODULE-2							
11	06.10.2025 Monday	**Module-2: Transistor at Low Frequencies:** Hybrid model, H-parameters for CE, CC and CB modes	**ICT**					
12	09.10.2025 Thursday	Mid-band analysis of single stage amplifier, Simplified hybrid model.	**ICT**					
13	10.10.2025 Friday	Analysis for CE, CB and CC(emitter voltage follower circuit) modes, Numerical solving.	Chalk & Talk					
14	13.10.2025 Monday	Millers Theorem and its dual, analysis for collector to base bias circuit and CE with un bypassed emitter resistance	ICT + Chalk & Talk					
15	14.10.2025 Tuesday	**Transistor frequency response:** General frequency considerations, Effect of various capacitors on frequency response	Chalk & Talk					
16	16.10.2025 Thursday	Miller effect capacitance, high frequency response, hybrid - pi model,	Chalk & Talk					
17	17.10.2025 Friday	CE short circuit current gain using hybrid-pi model,	Chalk & Talk					
18	21.10.2025 Tuesday	Multistage frequency effects Numerical Solving	ICT + Chalk & Talk					
19	23.10.2025 Thursday	Summary of Module-2, VTU QP Discussion, SRS Activity	ICT					
20	28.10.2025 Tuesday	Group Activity-2:	ICT					
IA-1: 24th, 25th and 27th October 2025								

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	MODULE 3							
21	30.10.2025 Thursday	**Module-3**: **Multistage amplifiers:** Cascade connection,	Chalk & Talk					
22	31.10.2025 Friday	Analysis for CE-CC mode, CE-CE mode	Chalk & Talk					
23	03.11.2025 Monday	CASCODE stage-unbypassed and bypassed emitter resistance modes.	ICT					
24	04.11.2025 Tuesday	Darlington connection using h-parameter model.	ICT+ Chalk & Talk					
25	06.11.2025 Thursday	**Feedback Amplifiers:** Classification of feedback amplifiers, concept of feedback, general characteristics of negative feedback amplifiers	Chalk & Talk					
26	07.11.2025 Friday	Input and output resistance with feedback of various feedback amplifiers	Chalk & Talk					
27	10.11.2025 Monday	Input and output resistance with feedback of various feedback amplifiers contd..	ICT+ Chalk & Talk					
28	11.11.2025 Tuesday	Analysis of different practical feedback amplifier circuits	ICT+ Chalk & Talk					
29	13.11.2025 Thursday	Summary of Module-3, VTU QP Discussion, SRS Activity	ICT					
30	14.11.2025 Friday	Group Activity-3:	ICT					

IA-II: 21st, 22nd & 24th November 2025

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Class No.	**Date planned (DD/MM)**	**Topics to be covered**	**TLP Planned**	**Class No.**	**Date planned (DD/MM)**	Topics to be covered	**TLP Planned**	**Remarks if any deviation**
	MODULE 4							
31	17.11.2025 Monday	**Module-4: Power Amplifiers:** Classification of power amplifiers, Analysis of class A amplifiers,.	ICT + Chalk & Talk					
32	18.11.2025 Tuesday	Analysis of Class B amplifiers.	ICT + Chalk & Talk					
33	20.11.2025 Thursday	Analysis of Class C and Class AB amplifiers.	Chalk & Talk					
34	25.11.2025 Tuesday	Distortion in power amplifiers, second harmonic distortion, harmonic distortion in Class B amplifiers, cross over distortion and elimination of cross over distortion	Chalk & Talk					
35	27.11.2025 Thursday	**Oscillators:** Concept of positive feedback, frequency of oscillation for RC phase oscillator,	Chalk & Talk					
36	28.11.2025 Friday	Wien Bridge oscillator, Tuned oscillator circuits.	ICT					
37	01.12.2025 Monday	Hartley oscillator, Colpitts's oscillator.	Chalk Talk					
38	02.12.2025 Tuesday	Crystal oscillator and its types.	Chalk Talk					
39	04.12.2025 Thursday	**Summary of Module-4, VTU QP Discussion, SRS Activity**	ICT					
40	05.12.2025 Friday	Group Activity-4	ICT					
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	MODULE 5							
41	08.12.2025 Monday	**Module-5:** Construction, working and characteristics of JFET (enhance and Depletion type)	Chalk & Talk					
42	09.12.2025 Tuesday	Construction, working and characteristics of MOSFET (enhance and Depletion type)	Chalk & Talk					
43	11.12.2025 Thursday	Biasing of JFET. Fixed bias configuration, self-bias configuration, voltage divider biasing.	ICT + Chalk & Talk					
44	12.12.2025 Friday	Biasing of MOSFET. Fixed bias configuration, self-bias configuration, voltage divider biasing Contd..	ICT + Chalk & Talk					
45	15.12.2025 Monday	**Analysis and design of JFET** (only common source configuration with fixed bias) amplifiers.	Chalk & Talk					
46	16.12.2025 Tuesday	Analysis and design of JFET (only common source configuration with fixed bias) amplifiers.	Chalk & Talk					
47	18.12.2025 Thursday	Analysis and design of MOSFET amplifiers.	ICT + Chalk & Talk					
48	19.12.2025 Friday	Analysis and design of JFET MOSFET amplifiers.	ICT + Chalk & Talk					
49	26.12.2025 Friday	**Summary of Module-5, VTU QP Discussion, SRS Activity**	ICT					
50	29.12.2025 Monday	Group Activity-5	ICT					

IA-III: 22nd,23rd & 24th Dec 2025
Last Working Day: January 4th 2026

	Course with Code: Analog Electronic Circuits –BEE303				Faculty: Shreeshayana R		Semester & Section: III	
Lab Session No.	**Date planned (DD/MM)**	**Topics to be covered**	**TLP Planned**	**Class No.**	**Date planned (DD/MM)**	Topics to be covered	**TLP Planned**	**Class No.**
	Lab Sessions							
1		Orientation Class: Introduction of course Module, Device Usage CRO, Singnal Generator, Multimeter, Power Supply..etc	Practical Session					
2		Experiments on series, shunt and double ended clippers and clampers.	Practical Session					
3		Design, simulation and Testing of Full wave – centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency.	Practical Session					
4		Static Transistor characteristics for CE, CB and CC modes and determination of h parameters	Practical Session					
5		Frequency response of single stage BJT and FET RC coupled amplifier and determination of half power points, bandwidth, input and output impedances	Practical Session					
6		Design and testing of BJT -RC phase shift oscillator for given frequency of oscillation.	Practical Session					
7		Design, simulation (MATLAB) and testing of Wien bridge oscillator for given frequency of oscillation.	Practical Session					
8		Design and testing of Hartley and Colpitt's oscillator for given frequency of oscillation.	Practical Session					
9		Determination of gain, input and output impedance of BJT Darlington emitter follower with and without bootstrapping	Practical Session					
10		Design and testing of Class A and Class B power amplifier and to determine conversion efficiency	Practical Session					

11		Design and simulation of Full wave – centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter using MATLAB. Determination of ripple factor, regulation and efficiency.	Practical Session					

	Activity	Planned	Actual	Remarks
1	Theory Classes	50		
2	Assignments/Quizzes/ Self study	5: SRS Group Activity:5		
3	Tutorials/ Extra classes			
4	Internal Assessments	3		
5	ICT based Teaching (% of usage in Curriculum)	35%		
6	Laboratory Session	11 Practical Sessions/ batch		
Planning			**Execution**	
Faculty Signature: 			**Faculty Signature:**	
HoD Signature: 			**HoD Signature:**	